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Advanced GeSi components for next-generation silicon photonics applications

SiPho-G

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Deliverable report

D5.1 – Specifications of transceiver modules and design report of Run #1

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About SIPHO-G

By developing 100Gbaud Germanium-Silicon (GeSi) Quantum-Confined Stark-Effect (QCSE) modulators and highly sensitive 100Gbaud avalanche photodetectors (APD), SIPHO-G will bring breakthrough optical modulation and photodetection capability to the world of Silicon Photonics. The newly developed compact, waveguide-coupled modulator and detector building blocks will be monolithically integrated in a high-yield cutting-edge 300mm Silicon Photonics platform, propelling the bandwidth density, power efficiency, sensitivity and complexity of silicon photonic integrated circuits to the next level. Supported by an elaborate simulation and design enablement framework, SIPHO-G will demonstrate an extensive set of application-driven prototypes across the O-band and C-band.

By bringing together the entire Silicon Photonics value chain, SIPHO-G will accelerate the development of next-generation co-packaged optics, long-haul optical communications, as well as emerging PIC applications such as optical neuromorphic computing, with performance levels of 4x-20x beyond current state of the art.

SIPHO-G consortium members

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Publishable summary

This deliverable report describes the design of the PIC circuits fabricated to test the performance of novel QCSE-based optical components and the flip chip assembly of PIC and EIC chips to implement co-packaged optical transceiver circuits targeting performance up to 100Gbaud. Using the early SIPHO-G technology of IMEC, a first generation of prototype components is designed and implemented as the first-step in a two-generation, two-step evaluation process.

In this report, three different demonstrator PIC circuits that are designed by imec are described. In addition, a first generation of an EIC circuit that contains the transceiver and receiver drivers for the PIC demonstrator circuits is designed by GF. The PIC demonstrators are designed to be assembled and tested together with the EIC, using flip-chip assembly.

Furthermore, 0.4Tbps DR4 transceiver circuits designed by Mellanox are described in this report. These designs serve as evaluation vehicles towards a 1.6Tbps DR8 transceiver implementation. Also a 16-QAM demonstrator based on FK-EAMs is designed by Mellanox towards the implementation of coherent transmitter circuits.

AUTH has designed several neuromorphic building blocks and layouts for early experimental validation of neuromorphic concepts.