

EUROPEAN COMMISSION

HORIZON 2020 PROGRAMME

TOPIC ICT-37-2020

**Advancing photonics technologies and application driven photonics
components and the innovation ecosystem**

GA No. 101017194

**Advanced GeSi components for next-generation silicon photonics
applications**

SiPho-G

Advanced GeSi components for next-generation silicon photonics applications

Deliverable report

**D5.1 – Specifications of transceiver modules and design
report of Run #1**

Disclaimer/ Acknowledgment



Copyright ©, all rights reserved. This document or any part thereof may not be made public or disclosed, copied or otherwise reproduced or used in any form or by any means, without prior permission in writing from the SIPHO-G Consortium. Neither the SIPHO-G Consortium nor any of its members, their officers, employees or agents shall be liable or responsible, in negligence or otherwise, for any loss, damage or expense whatever sustained by any person as a result of the use, in any manner or form, of any knowledge, information or data contained in this document, or due to any inaccuracy, omission or error therein contained.

All Intellectual Property Rights, know-how and information provided by and/or arising from this document, such as designs, documentation, as well as preparatory material in that regard, is and shall remain the exclusive property of the SIPHO-G Consortium and any of its members or its licensors. Nothing contained in this document shall give, or shall be construed as giving, any right, title, ownership, interest, license or any other right in or to any IP, know-how and information.

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 101017194. The information and views set out in this publication does not necessarily reflect the official opinion of the European Commission. Neither the European Union institutions and bodies nor any person acting on their behalf, may be held responsible for the use which may be made of the information contained therein.

About SIPHO-G

By developing 100Gbaud Germanium-Silicon (GeSi) Quantum-Confined Stark-Effect (QCSE) modulators and highly sensitive 100Gbaud avalanche photodetectors (APD), SIPHO-G will bring breakthrough optical modulation and photodetection capability to the world of Silicon Photonics. The newly developed compact, waveguide-coupled modulator and detector building blocks will be monolithically integrated in a high-yield cutting-edge 300mm Silicon Photonics platform, propelling the bandwidth density, power efficiency, sensitivity and complexity of silicon photonic integrated circuits to the next level. Supported by an elaborate simulation and design enablement framework, SIPHO-G will demonstrate an extensive set of application-driven prototypes across the O-band and C-band.

By bringing together the entire Silicon Photonics value chain, SIPHO-G will accelerate the development of next-generation co-packaged optics, long-haul optical communications, as well as emerging PIC applications such as optical neuromorphic computing, with performance levels of 4x-20x beyond current state of the art.

SIPHO-G consortium members



Document information

Deliverable No.	D5.1
Related WP	WP5
Deliverable Title	Specifications of transceiver modules and design report of Run #1
Deliverable Date	18 – May – 2021
Deliverable Type	Report
Lead Author	Dimitrios Kalavrouziotis (MELLANOX)
Co-Author(s)	Theoni Alexoudi, Apostolos Tsakyridis, George Giamougiannis, Miltiadis Moralis-Pegios, Konstantinos Fotiadis, Angelina Totovic, George Mourgias Alexandris and Nikos Pleros Dimitrios Velenis (imec), Yoojin Ban (imec)

Document history

Date	Revision	Prepared by	Approved by	Description
18.05.2022	1	Dimitrios Kalavrouziotis		First draft
01.09.2022	2	Dimitrios Kalavrouziotis		Proposed
23.09.2022	3	Dimitrios Kalavrouziotis		Reworked after review
26.09.2022	4	Dimitrios Kalavrouziotis	Morritz , Veroni Ballet (imec)	Approved

Dissemination level

PU	Public	
CO	Confidential, only for members of the consortium (including the Commission Services)	X

Publishable summary

This deliverable report describes the design of the PIC circuits fabricated to test the performance of novel QCSE-based optical components and the flip chip assembly of PIC and EIC chips to implement co-packaged optical transceiver circuits targeting performance up to 100Gbaud. Using the early SIPHO-G technology of IMEC, a first generation of prototype components is designed and implemented as the first-step in a two-generation, two-step evaluation process.

In this report, three different demonstrator PIC circuits that are designed by imec are described. In addition, a first generation of an EIC circuit that contains the transceiver and receiver drivers for the PIC demonstrator circuits is designed by GF. The PIC demonstrators are designed to be assembled and tested together with the EIC, using flip-chip assembly.

Furthermore, 0.4Tbps DR4 transceiver circuits designed by Mellanox are described in this report. These designs serve as evaluation vehicles towards a 1.6Tbps DR8 transceiver implementation. Also a 16-QAM demonstrator based on FK-EAMs is designed by Mellanox towards the implementation of coherent transmitter circuits.

AUTH has designed several neuromorphic building blocks and layouts for early experimental validation of neuromorphic concepts.